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09/716,977	11/20/2000	Alfred Earl Dunlop	13-6	1939

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EXAMINER	
ZHENG, EVA Y	

ART UNIT	PAPER NUMBER
2634	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/716,977	Applicant(s) DUNLOP ET AL.	
	Examiner Eva Yi Zheng	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-21,23-30,32-34* is/are rejected.

7)☒ Claim(s) *10,22,31,35,36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The objection to Fig. 3, block 370 has been withdrawn.

2. The objection to claim 17 has been withdrawn.

3. Claim rejection under 35 U.S.C. 112, first paragraph to claim 33 has been withdrawn due to applicant's amendment.

4. Applicant's arguments filed on May 17, 2004, have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – "as amended, require that the bias signal generate by a first PLL is not used to bias a second PLL in a second mode."

Examiner's response – Applicant is reminded that the Examiner is entitled to give the broadest reasonable interpretation to the language of claims. The recitation of claim 1: " a second PLL circuit generating a clock output signal, wherein said second PLL circuit is controlled by said bias signal generated by said first PLL circuit in a first mode and wherein said second PLL circuit has a second mode wherein said second PLL has an *initial* frequency determined by said bias signal and whereby said second PLL *substantially instantaneously* adjusts said clock output signal to phase changes of data in an input data stream without utilizing said bias signal." Phrase: "initial" and "substantially instantaneously" form contradiction for second mode signal operation. It is confusing and unclear of how does the second PLL instantaneously adjust to unbiased

signal while having a bias signal at the same time. Mittel et al. disclose a first PLL transmit a bias signal to a second PLL in a first mode. The second PLL generates a clock output signal at a second mode. Therefore, Mittel et al. meet all limitation as claimed.

5. Currently amended claims 1, 13, 15 and 33, the recitation: " a first phase-locked loop" is suggested to change to -- a first phase-locked loop (PLL)-- for clarity and to avoid insufficient antecedent basis of Claim rejection under 35 U.S.C. 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-9, 11-21, 23-30, and 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Mittel et al. (5,610,558).

a) Regarding claim 1, as shown in Fig.6, Mittel et al. disclose a clock recovery circuit, comprising:

a first phase-locked loop (PLL) circuit (block 202) for generating an oscillator signal having substantially the same frequency as a transmitter clock (Col 3, L 43-47) and for generating a bias signal (214); and

a second PLL circuit (block 206) generating a clock output signal (216), wherein said second PLL circuit is controlled by said bias signal generated by said first PLL circuit in a first mode (Col 4, L 1-4) and wherein said second PLL circuit has a second mode wherein said second PLL has an initial frequency determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream. (reference signal 147)

b) Regarding claims 2,14, and 27, as shown in Fig.1, Mittel et al. disclose a transition between said first and second modes is controlled by a transmission gate. (block 137)

c) Regarding claims 3, 15, and 28, as shown in Fig.1, Mittel et al. disclose a transition between said first and second modes is controlled by a switch. (block 137)

d) Regarding claims 4, 16, and 29, as shown in Fig.6, Mittel et al. disclose a transition between said first and second modes is controlled by a device that selectively imposes a bias current from said first PLL (signal 212) to said second PLL (signal 214).

e) Regarding claims 5, 17, and 30, Mittel et al. disclose a transition between said first and second modes is controlled by a device that selectively imposes a bias voltage from said first PLL to said second PLL. (Col 1, L26-29)

f) Regarding claims 6 and 18, Mittel et al. disclose the first PLL circuit is tuned to a local clock that operates at substantially the same frequency as a transmitter clock. (Col 3, L 43-47)

g) Regarding claims 7, 19, and 32, as shown in Fig.6, Mittel et al. disclose an elastic storage circuit for generating a jitter-compensated clock and data output. (block 208)

h) Regarding claims 8, 9, 20, and 21, Mittel et al. disclose the second mode is activated upon receipt of incoming data. (Col 4, L 1-11)

i) Regarding claims 11 and 23, Mittel et al. disclose the first and second PLLs operate at different frequencies in accordance with one or more predefined ratios. (Col 5, L 63- Col 6, L 2)

j) Regarding claims 12 and 24, Mittel et al. disclose the second PLL circuit generates said clock output signal using transmitted non-predetermined data. (Col 2, L59-61)

k) Regarding claim 13, Mittel et al. disclose a method for recovering a clock signal from an incoming data stream, comprising: as shown in Fig. 6,

tuning a first phase-locked loop (PLL) circuit (block 202) to a local clock signal (136) operating at substantially the same frequency as a transmitter clock (Col 3, L 43-47), wherein said first PLL circuit produces a bias signal (212);

applying said bias signal to a second PLL circuit (block 206) in a first mode, said second PLL circuit generating a clock output signal in said first mode having a frequency determined by said bias signal (216); and

removing said bias signal from said second PLL circuit in a second mode, wherein said second PLL circuit has an initial frequency in said second mode determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes in said incoming data stream in said second mode. (Col 4, L 1-4; reference signal 147)

l) Regarding claim 25, Mittel et al. disclose a clock recovery circuit, comprising: as shown in Fig. 6,

a first phase-locked loop (PLL) circuit (block 202) for generating an oscillator signal having substantially the same frequency as a transmitter clock (Col 3, L 43-47) and for generating a bias signal (212); and

a second PLL circuit (block 206) generating a clock output signal (216), wherein said second PLL circuit has an initial frequency determined by said bias signal (abstract) and wherein said second PLL circuit substantially instantaneously adjusts said clock output signal to phase changes of data of an input data stream when said input data stream is present. (signal 147; Col 4, L 1-4)

m) Regarding claim 26, as shown in Fig. 6, Mittel et al. disclose a clock recovery circuit, comprising:

first means for generating a first oscillator signal having substantially the same frequency as a transmitter clock (136, and 202; Col 3, L 43-47);

means for generating a bias signal (136,145, 302,306, 308,and 312);

second means for generating a clock output signal having an initial frequency determined by said bias signal and substantially instantaneously adjusting said clock

signal output signal to phase changes of data in an input data stream; (147, 316, 320, 322, and 326) and

means for selectively imposing said bias signal from said first means to said second means (125, 204, and 330).

n) Regarding claim 34, as shown in Fig. 6, Mittel et al. disclose the clock output signal (216) corresponds to phase changes of data of an input data stream (147) in a second mode when said input data stream is present.

Allowable Subject Matter

8. Claims 10, 22, 31, 35, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Yi Zheng whose telephone number is 703-305-8699. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

July 22, 2004

Eva Yi Zheng
Examiner
Art Unit 2634

SHUWANG LIU
PRIMARY EXAMINER